

26



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,074	11/19/2003	Peter Dean Swartz	GENSP052	1073
22434	7590	06/08/2006	EXAMINER	
BEYER WEAVER & THOMAS LLP			RICHER, AARON M	
P.O. BOX 70250			ART UNIT	
OAKLAND, CA 94612-0250			PAPER NUMBER	
			2628	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/707,074	Applicant(s) SWARTZ ET AL.	
	Examiner Aaron M. Richer	Art Unit 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 7-15, 18-25 and 29-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 7-15, 18-25, and 29-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed March 29, 2006 have been fully considered but they are not persuasive. Applicant argues that Gryskiewicz does not disclose that an output interlaced video signal has been adjusted for the specific analog display based upon any display device characteristics. It is noted that the receiver in Gryskiewicz automatically formats a video signal for an analog display device with frame rate of 30 Hz (col. 5, line 63-col. 6, line 5). These are display characteristics. It is noted that they are not adjustable display characteristics and that they do not take into account EDID information from the display, but they are display characteristics nonetheless.

2. Applicant further argues that Leyvi does not disclose a frame rate adjustment. Examiner notes that Leyvi is not used to anticipate this claim limitation, but for purposes of future reference, points out that Leyvi is concerned with conversion between progressive and interlaced formats (p. 3, section 0024). A conversion between 1080i and 980p would in most cases require a frame rate conversion (see http://en.wikipedia.org/wiki/High_definition_television for a description of different HDTV frame rates). 1080i60, as it is used typically in the US, is at 60 fields/sec. or 30 frames/sec. Progressive formats, such as 980p, or commonly used HDTV format 720p60, are typically at 60 frames/sec. The deinterlacer described by Leyvi combines the interlaced fields and effectively doubles the frame rate.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

Art Unit: 2628

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 4, 11, 15, and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 4, 15, and 24 recite that an output frame rate "can be" a number of values. This is indefinite because the language does not distinctly point out what the output frame rates are, simply what they are capable of being. The examiner has interpreted these claims as if the words "can be" were replaced with "is". MPEP 2106 states that "Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation".

6. Claim 11 is dependent on cancelled claim 6, and therefore it is not clear which claim claim 11 should be dependent on in the current set of claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 12-15, and 23-25 rejected under 35 U.S.C. 102(b) as being anticipated by Gryskiewicz (U.S. Patent 6,392,712).

9. As to claims 1, 12, and 23, Gryskiewicz discloses a configurable real time video processor arranged to provide a single synchronized video stream having a single

Art Unit: 2628

display video format to a display unit having an associated set of display attributes from a number of video streams of different video formats, comprising:

a number of ports each of which is configured to receive one of the video streams at a corresponding input video stream clock rate (fig. 1, elements 120, 130);

a number of adaptive image converter units each coupled to an associated one of the ports for converting the corresponding input video stream to a corresponding converted video stream having the single display video format that is based upon the set of display attributes (fig. 1; col. 8, lines 1-19; converter units from interlaced and progressive formats are combined to make a single output stream of interlaced format; this format has been chosen because the display attributes of the analog display, assumed to be a TV, require a 30 Hz frame rate);

and a frame rate conversion unit configured to synchronize each converted data stream to a selected output frame rate (col. 5, line 63-col. 6, line 5).

10. As to claims 2 and 13, Gryskiewicz discloses a format converter unit coupled to one of the ports arranged to convert a corresponding video stream to a progressive video stream, if needed (fig. 1; between elements 120 and 122, interlaced video is converted to progressive).

11. As to claims 3, 14, and 25, Gryskiewicz discloses a processor comprising:

an image compositor unit arranged to combine the converted data streams to form a composited data stream (fig. 1, element 156);

Art Unit: 2628

an image enhancer unit arranged to enhance the composited data stream to form an enhanced data stream (col. 8, lines 19-27; a "flicker" filter is used to enhance one of the streams, which in turn enhances the composited stream);

a display unit interface arranged process the enhanced data stream to form the display data (fig. 1, elements 158, 160);

and a memory unit bi-directionally coupled to each of the image converter units and the image compositor arranged to store selected portions of selected ones of the data streams from the image converter units and to provide the selected portions to the image compositor as needed (fig. 4, FIFO buffers are supplied as memory to store frames until the mixer is ready for them).

12. As to claims 4, 15, and 24, Gryskiewicz discloses a processor wherein the output frame is locked to any of the output video data stream clock rates (col. 5, line 63-col. 6, line 5; the output frame rate is locked to the input progressive stream rate).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

Art Unit: 2628

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 7, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz in view of Naegle (U.S. Publication 2004/0012577).

16. As to claims 7, 18, and 29, Gryskiewicz does not expressly disclose a processor wherein the display frame rate is a free running frame rate. Naegle, however, does disclose a video processor with a free running frame rate. The motivation for this is to provide a larger set of pixel clock frequencies for various formats (p. 1, paragraph 0014). It would have been obvious to one skilled in the art to modify Gryskiewicz to use a free running frame rate in order to support more diverse formats as taught by Naegle.

17. Claims 8, 19, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz in view of McKenna (U.S. Patent 6,915,528).

18. As to claims 8, 19, and 30, Gryskiewicz discloses
a video receiver port arranged to receive video data at a video clock rate (col. 5, line 63-col. 6, line 5);

Gryskiewicz further discloses a set-top box (col. 9, lines 36-45), which is often used for bi-directional communication to a network. Gryskiewicz does not disclose this specific use for a set-top box, however. McKenna, on the other hand, does disclose a user interface port arranged to receive user input commands inherently at a user interface clock rate and a network interface arranged bi-directionally connected to a

Art Unit: 2628

network arranged to transceive packet based data to and from the network (col. 7, lines 35-63). The motivation for this is to allow communications back to a broadcast center (col. 7, lines 44-53). It would have been obvious to one skilled in the art to modify Gryskiewicz to receive user input commands and connect to a network in order to communicate with a program source as taught by McKenna.

19. Claims 9, 20, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz.

20. As to claims 9, 20, and 31, Gryskiewicz does not disclose a processor as an integrated circuit. Official notice has been taken of the fact that graphics processors on integrated circuits are well-known in the art (see MPEP 2144.03). It would have been obvious to one skilled in the art to modify Gryskiewicz to use an integrated circuit in order to make the graphics processor smaller and reduce production costs.

21. Claims 10, 11, 21, 22, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gryskiewicz in view of Leyvi (U.S. Publication 2003/006752).

22. As to claims 10, 21, and 32, Gryskiewicz does not expressly disclose basing conversion on a set of Extended Display Identification Data (EDID) attributes. Leyvi, however, discloses a conversion process in which EDID is used to read attributes of a display (p. 3, paragraph 0025). The motivation for this is to easily determine whether a format is compatible with a display (p. 3, paragraph 0025). It would have been obvious to one skilled in the art to modify Gryskiewicz to read attributes of a display in EDID format in order to determine format compatibility as taught by Leyvi.

Art Unit: 2628

23. As to claims 11, 22, and 33, Gryskiewicz discloses a processor that comprises: an interlacer unit arranged to interlace a progressive scan image when the display unit is an interlaced type display unit (fig. 1, element 150). Although Gryskiewicz mentions displaying on a progressive display (col. 1, lines 39-52), the described embodiments of Gryskiewicz deal only with an interlaced display. Therefore, Gryskiewicz does not disclose a progressive scan bypass unit arranged to bypass the interlacer when the display unit is a progressive scan type display unit.

Leyvi, however, discloses a method in which EDID is read to determine whether to bypass a scan converter when a format matches a display (p. 3, paragraph 0025). Leyvi further discloses that progressive formats are used (p. 1, paragraph 0005). It is logical to then assume that if a signal in progressive format compatible with a display is passed to the invention of Leyvi, conversion will be bypassed. The motivation for this is the same as for any removal of any unnecessary graphics component: to save processing time and power. It would have been obvious to one skilled in the art to modify Gryskiewicz to bypass an unnecessary converter in order to save processing time and power as taught by Leyvi.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2628

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to clock rate and image format conversion in general:

U.S. Patent 5,555,097 to Joung

U.S. Patent 6,049,316 to Nolan

U.S. Patent 6,549,240 to Reitmeier

U.S. Publication 2004/0135924 to Conklin

U.S. Publication 2003/0038807 to Demos


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron M. Richer whose telephone number is (571) 272-7790. The examiner can normally be reached on weekdays from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2628

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AMR
6/2/06



Kee M. Tung
Primary Examiner